

# 1553 INTERFACE CARD

## User's Manual

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## 1553 INTERFACE CARD User's Manual

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### PREFACE

The 1553 INTERFACE CARD provides an intelligent interface between a PC/AT (286, 386 or 486) compatible computer and the MIL-STD-1553 data bus. The card is designed and manufactured by TEST SYSTEMS, Inc. in Phoenix, Arizona. TEST SYSTEMS, Inc. is an Arizona corporation, and has been specializing in MIL-STD-1553 test equipment since 1979.

### WARRANTY

TEST SYSTEMS, Inc., warrants the equipment manufactured by them to be free of defects in materials and workmanship for a period of 90 days from the date of shipment to the original purchaser. TEST SYSTEMS, Inc., will replace or repair any defective part or parts, free of charge, when the equipment is returned freight prepaid, and when examination reveals that the fault has not occurred because of misuse or abnormal conditions of operation. The current applicable rates will be charged for equipment repaired beyond the effective date of warranty or when abnormal usage has occurred. If requested, TEST SYSTEMS, Inc., will submit an estimate for charges before commencing repair.

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1.0 INTRODUCTION

The 1553 INTERFACE Card provides an intelligent interface between a PC/AT (286, 386 or 486) compatible computer and the MIL-STD-1553 data bus. It can operate as a Bus Controller (BC), Remote Terminal (RT), Bus Monitor (BM) or Remote Terminal/Bus Monitor (RT/M). This allows it to be used in developing, testing and simulating the MIL-STD-1553 bus functions from a personal computer.

1.1 Organization of Manual

Section 1 presents a brief introduction to the capabilities of the 1553 INTERFACE CARD. Section 2 provides electrical, environmental and physical specifications. Section 3 describes the board-level configuration of the card. Section 4 discusses the operation of the card. Section 5 explains how to program the card and use the software provided with the card.

1.2 Installation

The 1553 INTERFACE CARD fits in a 16 bit expansion slot of a PC (286, 386 or 486) compatible computer. The card has two 1553 data bus connectors (Trompeter BJ77) to allow it to operate on a dual standby redundant data bus network. The data bus connections may be either direct coupled or transformer coupled as set by the jumpers on the card (see section 3.1). The data bus connectors must be terminated properly into a resistive load or a bus network. The base I/O address must be set in the dip switch so as to not conflict with other I/O devices (see section 3.2). The SuMMIT may be configured through external pins or through internal control register bits (depending on the state of the \*LOCK pin). Jumpers are provided to set the external configuration pins of the SuMMIT (see section 3.3). A jumper needs to be installed for the desired interrupt if interrupts are to be enabled in the application software (see section 3.4). Following installation, it is recommended that the 1553 INTERFACE CARD Test Program be run to verify operation of the card (see section 5.1).

1.3 Operation

The 1553 INTERFACE CARD has a 1553 interface, up to 64K of 16 bit memory, control logic and PC interface circuitry. For the 1553 interface the card uses the SuMMIT from United Technologies Microelectronics Center to manage the critical functions of the MIL-STD-1553 protocol. The PC has full access and control of the SuMMIT. The SuMMIT internal registers, the full card memory (up to 64K) and the card status/control register are I/O mapped. The operation of the 1553 INTERFACE CARD is based on the combination of the information written into the 32 16 bit registers in the SuMMIT and the information written to various blocks in memory. For detailed operation of the SuMMIT refer to the SuMMIT Product Handbook from United Technologies Microelectronics Center, Inc., 1575 Garden of the Gods Road, Colorado Springs, CO 80907, (800)722-1575.

1.4 Software

Two programs are provided with the 1553 INTERFACE CARD; the 1553 INTERFACE CARD Test Program and the 1553 INTERFACE CARD Control Program.

The 1553 INTERFACE CARD Test Program is provided so that it can be run to verify that the 1553 INTERFACE CARD is functioning properly. The second purpose is to provide the user with a simple example to aid in developing custom application software. The Test Program is supplied in both object code and source code.

The 1553 INTERFACE CARD Control Program is a simple menu-driven program that allows the user to create and/or edit the files for the information written into the 32 16 bit registers in the SuMMIT and the information written to various blocks in memory to operate as a BC, RT, BM or RT/M. The Control Program allows the user to view and change the information in the 32 registers and memory during operation.

2.0 SPECIFICATIONS

Card Size: PC/AT short card, 4.8" high by 6.7" in length.

Memory: -8 8K words  
-16 16K words  
-32 32K words  
-64 64K words

Word Size: 16 bits

Communication Protocol: MIL-STD-1553 A or B

Data Bus: Dual Standby Redundant

Data bus Coupling: Transformer or Direct

Data Bus Connectors: Trompeter BJ77

Voltage: +5 V ± 5%

Current Drain: 1.8 Amps Maximum

Operating Temperature Range: 0 to 40 Degrees Celsius

Storage Temperature Range: -25 to +85 Degrees Celsius

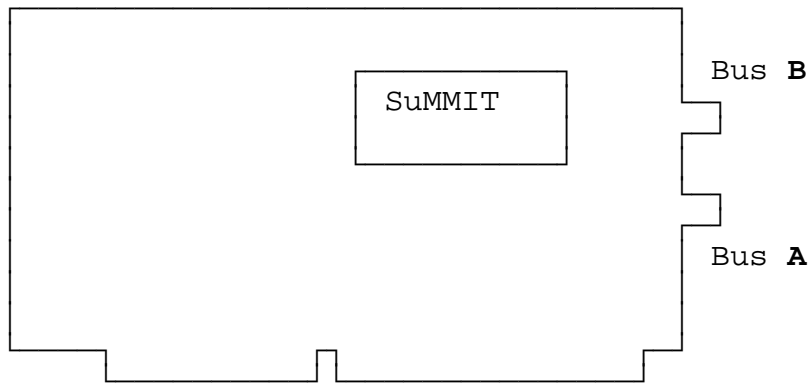
Relative Humidity: 10% to 90% Noncondensing

3.0 CARD CONFIGURATION

The user can configure the form of bus coupling (transformer or direct coupling), the base I/O address, optional SuMMIT configuration and the PC interrupt level on the 1553 INTERFACE CARD.

3.1 Bus Coupling

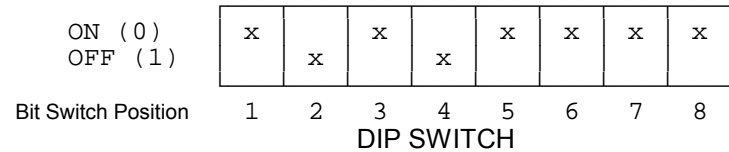
The 1553 INTERFACE CARD can be connected to a transformer coupled or direct coupled stub of the 1553 data bus. The user selects the desired form of coupling by configuring four jumpers on the board (J1, J2, J3 and J4) located near the data bus connectors. Each jumper position has three pins. To select transformer coupling, jumper the center pin to the pin marked T (left side) and to select direct coupling, jumper the center pin to the pin marked D (right side)



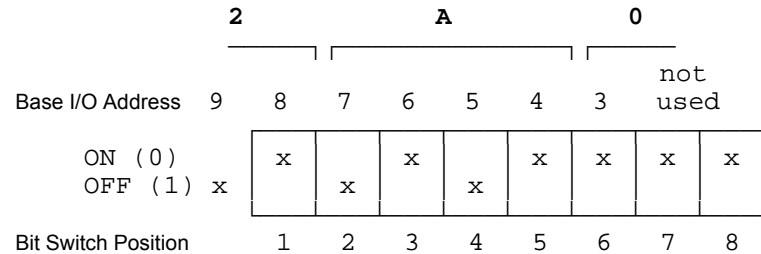
3.2 I/O Address

The 1553 INTERFACE CARD has a 16 bit interface designed to plug into the PC backplane. The card can be assigned any block of 8 I/O address from 0200h - 03FFh that is not being used by any other host processor function. The base address is selected by a dip switch. When there is an I/O address that matches the base I/O address of the dip switch, the data transceiver becomes tri-state enabled on the bus. I/O transfers are disabled when DMA transfers are in process.

The factory default base I/O address on the dip switch is 02A0h. Bit switch positions 7 and 8 are not used. The default dip switch settings for the base I/O address are as follows:



The I/O address contains ten address bits (A9-A0). The first seven address bits (A9-A3) define a block of eight addresses. For the default base I/O address of 02A0h this is the block 02A0h - 02A7h. Base I/O address bit 9 is a one and the dip switch base I/O address bits 8-3 are shown below. Note that switch position 1 is for I/O address 8. The default base I/O address (02A0h) is read in hexadecimal notation from the dip switch as follows:



The lower three address bits (A2-A0) define one of the eight unique addresses in the block. Only even addresses are used (address bit A0 is always zero) because 16 bits are transferred. If the default address of 02A0h is used, the following I/O addresses would be used for reading and writing the 1553 INTERFACE CARD:

(A3)	A2	A1	A0 (=I/O Address)	
0	0	0	0	(02A)0h Address Register (Write Only)
0	0	1	0	(02A)2h Memory (Read/Write)
0	1	0	0	(02A)4h SuMMIT Registers (Read/Write)
0	1	1	0	(02A)6h Status/Control Register (Read/Write)

3.3 Optional Configuration

The SuMMIT may be configured through external pins or through internal control register bits (depending on the state of the LOCK pin). Jumpers are provided to set the external configuration pins of the SuMMIT for LOCK, A/B STD, MODE M0 & M1 and the RT ADDRESS & PARITY. All pins except the RT ADDRESS & PARITY have jumpers on the solder side of the PWB which must be cut if the configuration is to be changed.

3.3.1 LOCK

The jumper position for the LOCK pin has three holes and is located below the SuMMIT. The factory default for the LOCK pin is unlocked with a jumper from 2 to 3. This allows the SuMMIT to be configured through the internal control registers. If the jumper on the solder side from 2 to 3 is cut and a jumper is installed from 1 to 2 the SuMMIT will be configured from the configuration pins and cannot be changed through the internal control registers.

3.3.2 A/B STD

The jumper position for the A/B STD pin has three holes and is located below the SuMMIT. The factory default for the A/B STD pin is B STD with a jumper from 1 to 2. To change the default to the A STD, cut the jumper on the solder side from 1 to 2 and installed a jumper from 2 to 3.

3.3.3 MODE M0 & M1

The jumper positions for the MODE M0 & M1 pins have three holes each and are located above the SuMMIT. The factory default for mode is BC. The MODE M0 & M1 pins have jumpers from 2 to 3. To change the default to another mode of operation, cut the jumpers on the solder side from 2 to 3 and installed jumpers as shown below:

<u>Mode</u>	<u>MODE M0 JUMPER</u>	<u>MODE M1 JUMPER</u>
BC	2 - 3	2 - 3
RT	1 - 2	2 - 3
BM	2 - 3	1 - 2
RT/M	1 - 2	1 - 2

3.3.4 RT ADDRESS & PARITY

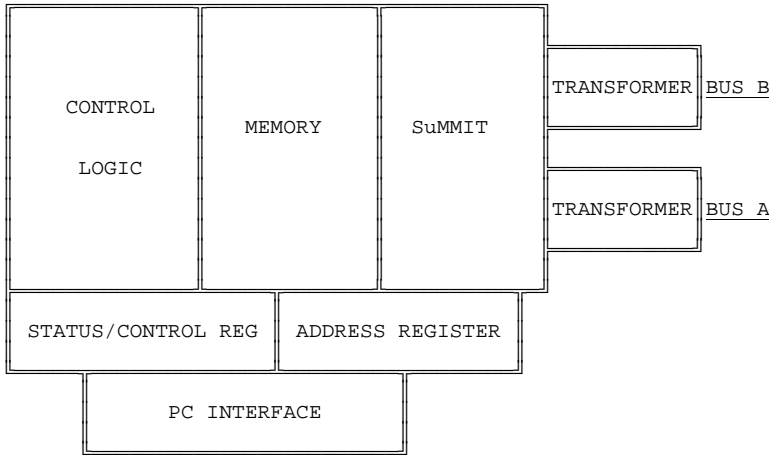
The jumper positions for the RT ADDRESS & PARITY pins have two holes each and are located above the SuMMIT. The default is a logic 'one' with no jumper installed. To set the default RT ADDRESS or PARITY bit to a logic 'zero' install a jumper for the desired bit.

3.4 Interrupt Level Selection

If interrupts are enabled in the application software, the desired interrupt level must be selected by installing a jumper at the desired IRQ position. Available selections are IRQ 3 - 7, 9 - 12, 14 and 15. Only one jumper is to be installed and the selected IRQ must not be used by any other device in the computer.

4.0 CARD OPERATION

A Block Diagram of the 1553 INTERFACE CARD is shown below. A brief description of the operation is given in the following sections.



4.1 PC Interface

The operation of the 1553 INTERFACE CARD is controlled by transferring information to and from Memory, the internal registers in the SuMMIT and a Status/Control Register. An Address Register (Counter) is also provided to facilitate block transfers. All PC transfers are through I/O ports and are 16 bit words where the lsb is bit 0 and the msb is bit 15. The card is assigned a block of 8 I/O address from 0200h - 03FFh that is not being used by any other host processor function. The base address is selected by a dip switch. Since the transfers are 16 bits, only the 4 even I/O addresses are used. The 4 I/O address ports are assigned as follows:

I/O Address	Port	Function
XXX0(or 8)	0	Address Register (Write Only)
XXX2(or A)	2	Memory (Read/Write)
XXX4(or B)	4	SuMMIT Registers (Read/Write)
XXX6(or E)	6	Status/Control Register (Read/Write)

To transfer data to or from Memory or the SuMMIT Registers, an address is first written to the Address Register (I/O write to Port 0 or I/O Address XXX0). Then data is read from or written to Memory (Port 2) or the SuMMIT Registers (Port 4) at the location specified by the Address Register. Each time there is a read or write to Memory or the SuMMIT Registers the Address Register is automatically incremented. This allows blocks of consecutive data to be transferred without having to write the address for each word.

The Status/Control Register provides additional information and control for the operation of the card. An I/O read of Port 6 (I/O Address XXX6) provides the card Status. An I/O write to Port 6 (I/O Address XXX6) provides the card Control. The Status Definition and Control Function for the 16 bits in the Status/Control Register are as follows:

Bit	Status Definition	Control Function
15	0	N/A
14	0	N/A
13	0	N/A
12	0	N/A
11	0	N/A
10	0	N/A
9	0	Reset Timer Resolution
8	Timer Resolution	Set Timer Resolution
7	Ready Status	Master Reset SuMMIT
6	Terminal Active Status	N/A
5	0	Reset Subsystem Flag
4	Subsystem Flag	Set Subsystem Flag
3	0	Reset Interrupt Enable
2	Interrupt Enable	Set Interrupt Enable
1	You Fail Interrupt	Reset You Fail Interrupt
0	Message Interrupt	Reset Message Interrupt

4.1.1 Description of Status Register Bits

The Message Interrupt signal from the SuMMIT is a 125 ns pulse which is latched and provided in bit 0. The You Fail Interrupt signal from the SuMMIT is a 125 ns pulse which is latched and provided in bit 1. Once an interrupt is latched the status bit will remain high until it is reset by writing the appropriate bit in the Control Register. The PC interrupts can be enabled

or disabled by writing to the Control Register and a 'one' in bit 2 of the Status Register indicates the PC interrupts are enabled.

When the card is used as an RT, the Subsystem Flag bit in the 1553 RT status word can be set by writing to a SuMMIT Register or by writing to the Control Register and a 'one' in bit 4 of the Status Register indicates the Subsystem Flag has been set from the Control Register.

Bit 6 provides Terminal Active status from the SuMMIT which indicates that the SuMMIT is actively processing a 1553 command. Bit 7 provides Ready status from the SuMMIT which indicates that the SuMMIT has completed initialization or BIT, and regular execution may begin.

Bit 8, Timer Resolution, indicates the frequency selected and applied to the Timer Clock input to the SuMMIT. When Timer Resolution is a 'zero' the Timer Clock frequency is 250 KHz yielding a timer resolution of 4 us. When Timer Resolution is a 'one' the Timer Clock frequency is approximately 976 Hz yielding a timer resolution of 1,024 us. Note that the internal frequency of 24 MHz yields a timer resolution of 64 us.

#### 4.1.2 Description of Control Register Bits

When a 'one' is written to a bit in the Control Register, the function of that bit is executed. When writing to the Control Register, if both the Set and the Reset bits are 'one' for Interrupt Enable, Subsystem Flag and Timer Resolution, the function is reset.

#### 4.1.3 Interrupts

The SuMMIT can be configured to generate two different interrupts during operation. The interrupts are 125 ns pulses which are latched in the card Status Register. The interrupts will interrupt the PC if interrupts are enabled (card status bit 2 is 'one') and a jumper is installed for the desired PC interrupt level (IRQ 3-7, 9-12, 14 or 15). Note that only one jumper is to be installed and the selected IRQ must not be used by any other device in the computer. Once the PC is interrupted, the card Status Register can be read to determine which interrupt caused the interrupt. The interrupt must be reset by writing to the Control Register. If interrupts are not enabled (card status bit 2 is 'zero'), the interrupts can be polled by reading the card Status Register. Interrupt Enable is set or reset by writing to the Control Register.

## 4.2 SuMMIT Operation

The SuMMIT operation is based on the combination of the information written into the 32 16 bit registers in the SuMMIT and the information written to various blocks in memory. The SuMMIT can be set up to operate as a Bus Controller (BC), Remote Terminal (RT), Bus Monitor (BM) or Remote Terminal/Bus Monitor (RT/M). For detailed operation of the SuMMIT refer to the [SuMMIT Product Handbook](#) from United Technologies Microelectronics Center, Inc., 1575 Garden of the Gods Road, Colorado Springs, CO 80907, (800)722-1575.

5.0 SOFTWARE SUPPORT

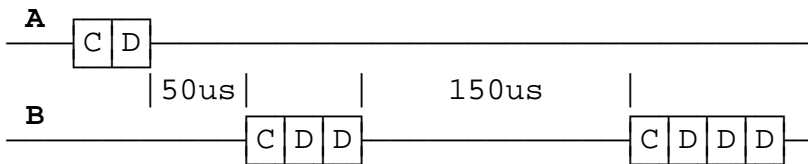
Two programs are provided with the 1553 INTERFACE CARD; the 1553 CARD Test Program and the 1553 INTERFACE CARD Control Program. In addition, the 1553 INTERFACE CARD DOS Support Library is provided and the 1553 INTERFACE CARD Windows DLL is available.

5.1 1553 INTERFACE CARD Test Program

The purpose of the 1553 INTERFACE CARD Test Program is twofold. First, the program is provided so that it can be run to verify that the 1553 INTERFACE CARD is functioning properly. The second purpose is to provide the user with a simple example to aid in developing custom application software. The Test Program is supplied in both object code and source code.

5.1.1 1553 INTERFACE CARD Verification

Install the 1553 INTERFACE CARD in the PC following the installation information given in section 1.2. Install a resistive load on the data bus connectors of 70 ohms for Transformer coupled or 35 ohms for Direct coupled. Connect a scope probe across each of the load resistors. Run the Test Program and observe the waveforms on Bus A (lower connector) and Bus B (upper connector) for the following patterns:



5.1.2 1553 INTERFACE CARD Programming

The 1553 INTERFACE CARD has a Status/Control Register, an Address Register (counter), 32 16 bit registers in the SuMMIT and up to 64 K 16 bit words of memory that can be accessed with any I/O port input or output function. The Test Program provides a simple example to illustrate initialization and operation of the card.

5.2 1553 INTERFACE CARD Control Program

The 1553 INTERFACE CARD Control Program provides convenient control of the capability of the 1553 INTERFACE CARD through a simple menu-driven program. The user can create and/or edit the files for the information written into the 32 16 bit registers in the SuMMIT and the information written to various blocks in memory to operate the card as a BC, RT or BM. The Control Program allows the user to view and change the information in the registers and memory during operation.

The operation of the Control Program is described in detail in the 1553 INTERFACE CARD CONTROL PROGRAM User's Manual.

5.3 1553 INTERFACE CARD DOS Support Library

The DOS Support Library is a static link library that provides the basic support for programming in DOS to operate the 1553 INTERFACE CARD. Examples are provided to illustrate the use of the functions in the library.

5.4 1553 INTERFACE CARD Windows DLL

The 1553 INTERFACE CARD Windows DLL is a Dynamic Link Library (DLL) that provides the basic support for programming in Windows or LabView to operate the card. Examples for Windows and LabView are provided to illustrate the use of the functions in the DLL. The Windows DLL is sold separately.